SEMICONDUCTOR DEVICE USING CURRENT MIRROR CIRCUIT

[0001] This application claims priority to prior application JP 2002-280855, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION:

[0002] The present invention relates to a semiconductor device which uses current mirror circuits to generate CMOS level signals from small amplitude signals.

[0003] With the recent trend toward higher speed and reduced power consumption in microprocessors, there has been an increasing demand for DRAMs featuring higher-speed data transfer and DRAMs permitting reduced power consumption. To meet customers' needs, efforts have been focused on the development of 288 Mbit Direct Rambus DRAM chips capable of achieving both higher-speed operations and reduced power consumption. In order to meet the customers' needs described above, it is necessary to accomplish lower internal voltages of peripheral circuits (DLL circuit and logic circuit) which are most responsible for current drain. However, the DLL circuit of the peripheral circuits is required to operate the transistors of a current mirror circuit in saturation regions to generate stable-duty clocks (duty=50±1%). For this reason, the supply voltage of the DLL circuit must be set to at least 2.0 V.

[0004] Meanwhile, the supply voltage of a logic circuit can be dropped to an extent that does not affect the characteristics of the circuit or its high-speed operation. In the development efforts, the supply voltage of the DLL circuit should be set to 2.0 V and the supply voltage of the logic circuit should be set to 1.8 V or less to satisfy the characteristics of both circuits

and to realize higher-speed operation and reduced power consumption at the same time. This requires the re-designing of the level converting circuit for transferring signals between the DLL circuit and the logic circuit.

[0005] Fig. 1 is an example of a conventional level converting circuit (refer to, for example, Japanese Unexamined Patent Publication No. 11-242204).

[0006] The conventional level converting circuit performs the level conversion of small amplitude signals CLKI and CLKIB in a DLL circuit into a CMOS level signal CLKO and supplies the CMOS level signal CLKO to the logic circuit. In this case, the supply voltages of the DLL circuit and the logic circuit share the same potential.

[0007] In the conventional circuit shown in Fig. 1, if the small amplitude signal CLKI is high and the small amplitude signal CLKIB is low, then an NMOS transistor N1 is ON, while an NMOS transistor N2 is OFF, and the NMOS transistor N1 causes currents to flow from a node st1b to common. This causes the potential at the node st1b to fall from the high level to the low level, thus turning PMOS transistors P1, P3 and P6 ON.

[0008] The switching of the potential of the node st1b from the high level to the low level causes the PMOS transistor P6 to pass currents from VDDA to a node co, thereby switching the voltage level of the node co from low to high. The switching of the potential of the node co from low to high causes a node cob to be switched from high to low and the CMOS level signal CLKO from low to high.

[0009] If the small amplitude signal CLKI is low and the small amplitude signal CLKIB is high, then the NMOS transistor N1 is OFF, while the NMOS transistor N2 is ON, and the NMOS transistor N2 causes currents to flow from a node st1 to common. This causes the potential at the node st1 to fall from high to low, turning PMOS transistors P2, P4 and P5 ON.

[0010] Thus, the potential of a node coma is switched from low to high,

NMOS transistors N3 and N4 are turned ON, and the potential of the node co is switched from high to low. The switching of the potential of the node co from high to low causes the node cob to be switched from low to high, and the CMOS level signal CLKO to be switched from high to low.

[0011] In the conventional circuit, the supply voltages of the DLL circuit and the logic circuit share the same potential, so that no particular attention has been paid to the potential difference in the supply voltages of the DLL circuit and the logic circuit. If, however, the power sources of the DLL circuit and the logic circuit belong to separate systems, as in this case, then changes in the potential difference between both power sources cause mismatch between the potential of the node co shown in Fig. 2 and the logic threshold of an input of the inverter, resulting in a deteriorated duty, as shown in Fig. 3. The result is illustrated in Fig. 4.

[0012] Referring to Fig. 4, when the supply voltage of the DLL circuit is set to VDDA=2.0 V, and the supply voltage of the logic circuit (VDD) is changed from 2.0 V to 1.6 V, the duty is mismatched by about 3.5%. The amount of the mismatch exceeds a design target value of 1% or less. Thus, even if the duty is adjusted in the DDL circuit, the mismatch of the duty inevitably occurs when the signal is given to the logic circuit. As a result, the adjustment is meaningless.

SUMMARY OF THE INVENTION:

[0013] It is therefore an object of the present invention to provide a semiconductor device which is capable of producing stable CMOS level signals (duty=50±1%) even when the supply voltages of a DLL circuit and a logic circuit fluctuate.

[0014] According to the present invention, there is provided a semiconductor device including a first current mirror circuit combining an analog power source and a digital power source to receive a small amplitude

signal and a constant-voltage input signal, a second current mirror circuit for receiving a signal output from the first current mirror circuit and for level-converting the signal from analog power source to digital power source, a first node provided in the first current mirror circuit, a second node provided in the second current mirror circuit, and an inverter circuit for receiving a signal output on the basis of the voltage levels of the first node and the second node and for outputting a CMOS level signal.

[0015] The first current mirror circuit is preferably structured by a plurality of first PMOS transistors and a plurality of first NMOS transistors. The second current mirror circuit is preferably structured by a pair of second PMOS transistors and a pair of second NMOS transistors. The inverter circuit is preferably structured by a pair of third PMOS transistors and a pair of third NMOS transistors.

[0016] Preferably, the number of the first PMOS transistors is six, and the number of the first NMOS transistors is four.

[0017] The digital power source of the first current mirror circuit and the digital power source of the inverter circuit may be set at the same potential.

[0018] With this structure, the potential of an input signal to the inverter circuit preferably coincides with the logic threshold of an input of the inverter circuit.

[0019] The potential of the input signal and the logic threshold are set to coincide with each other so as to set a duty within the range of a predetermined target value.

[0020] The semiconductor device is, for example, a direct Rambus DRAM.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0021] Fig. 1 is a diagram showing a conventional level converting circuit;

[0022] Fig. 2 is another diagram showing the conventional level

converting circuit;

[0023] Fig. 3 illustrates the duty deteriorated by the mismatch between the potential of a node co shown in Fig. 5 and the logic threshold of the input of the inverter;

[0024] Fig. 4 is a graph illustrating the results of the improvement shown in Fig. 6;

[0025] Fig. 5 shows a level converting circuit according to the present invention;

[0026] Fig. 6 illustrates the match between the potential of the node co shown in Fig. 1 and the logic threshold of the input of the inverter, which makes it possible to prevent the duty from deteriorating; and

[0027] Fig. 7 is a graph illustrating the results of the mismatch shown in Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS:

[0028] An embodiment according to the present invention will be described in conjunction with the accompanying drawings.

[0029] Referring to Fig. 5, description will be made of a circuit structure of an embodiment according to the present invention.

[0030] The level converting circuit according to the present invention is capable of converting small amplitude signals CLKI and CLKIB into a CMOS level signal CLKO (duty=50±1%) with a stable duty ratio even when the supply voltage levels of a DLL circuit and a logic circuit fluctuate (refer to Fig. 6). The level converting circuit is applied to, for example, a direct Rambus DRAM.

[0031] Unlike the conventional circuit shown in Fig. 1, the level converting circuit according to the present invention comprises a current mirror circuit A having PMOS transistors P1, P2, P3, P4, P5 and P6 and NMOS transistors N1, N2, N3, N4 and NC, a current mirror circuit B having

PMOS transistors P9 and P10 and NMOS transistors N7 and N8, and an inverter circuit having PMOS transistors P7 and P8 and NMOS transistors N5 and N6.

[0032] The major difference from the conventional circuit shown in Fig. 1 is the addition of the current mirror circuit B. The use of the current mirror circuit B makes it possible to match the potential of the node co shown in Fig. 5 with the logic threshold of the input of the inverter, thus preventing the deterioration of the duty, as shown in Fig. 6. Thus, the duty mismatch is extremely small, as compared with that in the conventional circuit. The effect is shown in Fig. 7.

[0033] The operation of the circuit according to the embodiment of the invention will now be explained.

[0034] Referring to Fig. 5, if a small amplitude signal CLKI is high and a small amplitude signal CLKIB is low, then an NMOS transistor N1 is ON, while an NMOS transistor N2 is OFF, and the NMOS transistor N1 causes currents to flow from a node st1b to common. This causes the potential at the node st1b to be fall from the high level to the low level, turning PMOS transistors P1, P3 and P9 ON.

[0035] The switching of the potential of the node st1b from the high level to the low level causes the PMOS transistor P9 to pass currents from VDDA to a node comb to switch the voltage of the node comb from low to high.

[0036] The switching of the potential of the node comb from low to high causes a node combb to switch from high to low. Thus, the node co switches from low to high, and a node cob switches from high to low. This causes the CMOS level signal CLKO to switch from low to high. Conversely, if the small amplitude signal CLKI is low and the small amplitude signal CLKIB is high, then the NMOS transistor N1 is OFF, while the NMOS transistor N2 is ON, and the NMOS transistor N2 causes currents to flow from a node st1 to common. This causes the potential at the node st1 to fall

from high to low, turning PMOS transistors P2, P4 and P5 ON.

[0037] This causes the potential of a node coma to switch from low to high and the NMOS transistors N3 and N4 turn ON so as to switch the potential of the node co from high to low. The switching of the potential of the node co from high to low causes the node cob to switch from low to high and the CMOS level signal CLKO to switch from high to low. An NMOS transistor NC constitutes a constant-current source circuit and has a constant voltage VCN applied to its gate.

[0038] As described above, according to the present invention, even if the supply voltages of a DLL circuit and a logic circuit fluctuate (VDDA>VDD), the potential of a node (co) and the logic threshold of the input of an inverter match, thus preventing the duty from deteriorating. This makes it possible to generate the CMOS level signal CLKO having a duty of 50±1%.

[0039] Moreover, the supply voltage of the logic circuit can be reduced, allowing current drain to be reduced accordingly.

[0040] While the present invention has thus far been disclosed in conjunction with several embodiments thereof, it will be readily possible for those skilled in the art to put the present invention into practice in various other manners.